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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/035,444

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Fumikazu Yamaki

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05/18/2004

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EXAMINER

TRAN, TAN N

ART UNIT

PAPER NUMBER

2826

DATE MAILED: 05/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/035,444	Applicant(s) YAMAKI ET AL.	
	Examiner TAN N TRAN	Art Unit 2826	

-- **Th MAILING DATE of this communication appears on the cover sheet with the correspond nce address --**
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on amendment filed on 03/24/04.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-10 and 12-27 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-10 and 12-27 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-8,10,15,16 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Shibasaki et al. (5,430,310) in view of Ishikawa (6,294,446).

With regard to claims 1,2,16, Shibasaki et al. discloses a high power semiconductor FET device for a radio communication system, comprising: a compound semiconductor GaAs substrate 1 having a resistivity of 10^7 ohm-cm at least at surface thereof or higher; a buffer layer 2 formed on the compound semiconductor substrate 1 wherein the buffer layer 2 having lattice matching with InAs material; and an active layer 3 formed on the buffer layer 2 and having a high power active element for radio communication formed therein. (Note lines 41,42, column 16; and lines 37,38, column 17; lines 4,5, column 19, figs. 3,14 of Shibasaki et al.).

Shibasaki et al. does not disclose the buffer layer is a super lattice.

However, Ishikawa discloses a super lattice buffer layer 32 formed on the compound semiconductor substrate 31. (Note fig. 1 of Ishikawa).

Therefore, it would have been obvious to one of ordinary skill in the art to form the Shibasaki et al.'s device having the buffer layer is a super lattice such as taught by Ishikawa in order to reduce threading dislocations.

With regard to claim 3, Shibasaki et al. and Ishikawa disclose all the claimed subject matter except for the active layer is formed at a position within 5.0 micrometer from a surface of the compound semiconductor substrate. However, it would have been obvious to one of ordinary skill in the art to form the active layer is formed at a position within 5.0 micrometer from the surface of the compound semiconductor substrate in order to maintain the lattice matching between the semiconductors and the sapphire substrate.

With regard to claims 4,5, Shibasaki et al. and Ishikawa disclose all the claimed subject matter except for an electrode formed on another surface of the compound semiconductor substrate and not electrically connected to the semiconductor device. However, it would have been obvious to one of ordinary skill in the art to form an electrode formed on another surface of the compound semiconductor substrate and not electrically connected to the semiconductor device in order to provide potential for semiconductor device.

With regard to claim 6, Shibasaki et al. and Ishikawa disclose all the claimed subject matter except for the electrode layer is connected to one power supply potential of the semiconductor device. However, it would have been obvious to one of ordinary skill in the art to connect the lower electrode layer to one power supply potential of the semiconductor device in order for the device to operate.

With regard to claim 7, Shibasaki et al. discloses a source electrode 5 and drain electrode 7 formed on the active layer 3, separated from each other so as to establish a channel region, and a gate electrode 6 formed above the channel region. (Note fig. 9 of Udagawa et al.)

With regard to claim 8, Shibasaki et al. discloses the active layer 3 has 2 dimensional electron gasses. (Note lines 17,18, and lines 55-59, column 1 of Shibasaki et al.).

With regard to claim 10, Shibasaki et al. and Ishikawa disclose all the claimed subject matter except for the compound semiconductor substrate has resistivity more than 1.0×10 Ohm-cm in total. However, it would have been obvious to one of ordinary skill in the art to form the compound semiconductor substrate has resistivity more than 1.0×10 Ohm-cm in total in order to reduce the resistance of semiconductor substrate. Note (lines 52-54, column 9, fig. 3 of Shibasaki et al.) is cited to support for the well-know position.

With regard to claim 15, Shibasaki et al. discloses the active layer 3 is doped with Si to a concentration of $1 \times 10^{16} \text{ cm}^{-3}$ to $5 \times 10^{18} \text{ cm}^{-3}$. (Note lines 60-68, column 13, fig. 3 of Shibasaki et al.).

Claim 9 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Shibasaki et al. (5,430,310) in view of Ishikawa (6,294,446) and further in view of Usagawa et al. (5,373,191).

With regard to claim 9, Shibasaki et al. and Ishikawa do not disclose the active layer comprises: a collector layer of a first conducting type; a base layer of a second conducting type formed on the collector layer; an emitter layer of the first conducting type formed on the base layer.

However, Usagawa et al. (5,373,191) discloses the active layer comprises: an n-type collector layer 101, a p-type base layer 103, and an n-type emitter layer 105. (Note figs. 12a-12c and embodiment 6 in column 10 of Usagawa et al.).

Therefore, it would have been obvious to one of ordinary skill in the art to form the Shibasaki et al. and Ishikawa's device having the active layer comprises: an n-type collector layer, a p-type base layer, and an n-type emitter layer such as taught by Usagawa et al. in order for forming the bipolar transistor.

Claims 12-14,17-19 rejected under 35 U.S.C. 103(a) as being unpatentable over Shibasaki et al. (5,430,310) in view of Ishikawa (6,294,446) and further in view of Udagawa et al. (6,462,361).

With regard to claims 12-14, Shibasaki et al. and Ishikawa do not disclose the buffer layer has a GaAs/AlGaAs super lattice, the GaAs/AlGaAs super lattice structure includes undoped GaAs layers having carrier concentration less than $1 \times 10^5 \text{ cm}^{-3}$ and undoped AlGaAs layers having carrier concentraion less than $1 \times 10^{16} \text{ cm}^{-3}$.

However, Udagawa et al. discloses a buffer layer 302-1 formed on the compound semiconductor GaAs substrate 301 wherein the buffer layer 302-1 having AlGaAs/GaAs super lattice structure; the AlGaAs/GaAs super lattice structure includes undoped GaAs layers 302b having carrier concentration $7 \times 10^{13} \text{ cm}^{-3}$ and undoped AlGaAs layers ^{302a} having carrier concentraion $1 \times 10^{14} \text{ cm}^{-3}$ (Note lines 41-46, 49-52, column 22, fig. 3 of Udagawa et al.).

Therefore, it would have been obvious to one of ordinary skill in the art to form the Shibasaki et al. and Ishikawa's device having the buffer layer is a super lattice such as taught by Udagawa et al. in order to reduce the leakage current from channel layer of the device.

With regard to claims 17-19, Udagawa et al., Shibasaki et al. and Ishikawa disclose all the claimed subject matter except for the super lattice buffer layer inhibits electrical field concentration in the active layer or inhibits electrons leaking from the active layer from accumulating at the interface between the low-resistance substrate and the buffer layer or inhibits domain generation in the buffer layer under high power operating conditions. However, in reference to the claim language referring to the function of the super lattice buffer layer, intended use and other types of functional language must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In a claim drawn to a process of making, the intended use must result in a manipulative difference as compared to the prior art. In re Casey, 152 USPQ 235 (CCPA 1967); In re Otto, 136 USPQ 458, 459 (CCPA 1963).

Claims 10,20-22,24-27 rejected under 35 U.S.C. 103(a) as being unpatentable over Udagawa et al. (6,462,361) (of record).

With regard to claims 10,20,24, Udagawa et al. discloses a compound semiconductor GaAs substrate 301 having a resistivity of $3 \times 10^7 \text{ } \Omega \cdot \text{cm}$; a buffer layer 302-1 formed on the compound semiconductor GaAs substrate 301 wherein the buffer layer 302-1 having AlGaAs/GaAs super lattice structure; and an active layer 303(304) formed

on the buffer layer 302-1 and having a high power active element formed therein. (Note lines 41-46, column 22, fig. 3 of Udagawa et al.).

Udagawa et al. discloses all the claimed subject matter except for the compound semiconductor substrate has resistivity more than 1.0×10 Ohm-cm in total. However, it would have been obvious to one of ordinary skill in the art to form the compound semiconductor substrate has resistivity more than 1.0×10 Ohm-cm in total in order to reduce the resistance of semiconductor substrate. (Note lines 52-54, column 9, fig. 3 of Shibasaki et al. (5,430,310)) is cited to support for the well-know position.

With regard to claims 21,22, Udagawa et al. discloses the AlGaAs/GaAs super lattice structure includes undoped GaAs layers 302b having carrier concentration $7 \times 10^{13} \text{ cm}^{-3}$ and undoped AlGaAs layers ^{302a} having carrier concentraion $1 \times 10^{14} \text{ cm}^{-3}$ (Note lines 49-52, column 22, fig. 3 of Udagawa et al.).

With regard to claims 25-27, Udagawa et al. discloses the super lattice buffer layer 302-1 is disposed between the compound semiconductor substrate 301 and the active layer 303. (Note fig. 3 of Udagawa et al.). Udagawa et al. discloses all the claimed subject matter except for the super lattice buffer layer inhibits electrical field concentration in the active layer or inhibits electrons leaking from the active layer from accumulating at the interface between the low-resistance substrate and the buffer layer or inhibits domain generation in the buffer layer under high power operating conditions. However, in reference to the claim language referring to the function of the super lattice buffer layer, intended use and other types of functional language must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is

capable of performing the intended use, then it meets the claim. In a claim drawn to a process of making, the intended use must result in a manipulative difference as compared to the prior art. In re Casey, 152 USPQ 235 (CCPA 1967); In re Otto, 136 USPQ 458, 459 (CCPA 1963).

Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Udagawa et al. (6,462,361) (of record) in view of Shibasaki et al. (5,430,310).

With regard to claim 23, Udagawa et al. does not disclose the active layer is doped with Si to a concentration of $1 \times 10^{17} \text{ cm}^{-3}$.

However, Shibasaki et al. discloses the active layer 3 is doped with Si to a concentration of $1 \times 10^{16} \text{ cm}^{-3}$ to $5 \times 10^{18} \text{ cm}^{-3}$. (Note lines 60-68, column 13, fig. 3 of Shibasaki et al.).

Therefore, it would have been obvious to one of ordinary skill in the art to form the Udagawa et al.'s device having the active layer is doped with Si to a concentration of $1 \times 10^{17} \text{ cm}^{-3}$ such as taught by Shibasaki et al. in order to increase the conductivity of active layer.

Response to Arguments

2. Applicant's arguments filed 3/24/04 have been fully considered but they are not persuasive.

It is argued, at page 9 of the remarks, that "Shibasaki does not teach a buffer layer that is a super lattice". However, fig. 1 of Ishikawa does show a super lattice buffer layer 32 formed on the compound semiconductor substrate 31.

It is argued, at pages 11,12,14,15 of the remarks, that "The combination of Shibasaki and Ishikawa is improper because there is no suggestion or motivation supporting the combination";

“the skilled artisan in view of Shibasaki requiring a simple buffer layer, would have no motivation to look to art requiring a super-lattice buffer layer, i.e. Ishikawa. Likewise, the skilled artisan in view of Ishikawa requiring a super-lattice buffer layer, would have no motivation to look to art requiring a simple buffer layer, i.e, Shibasaki”; “even if Shibasaki and Ishikawa were proper, there is no motivation to modifying by substituting the super-lattice buffer layer of Ishikawa for the simple buffer layer of Shibasaki. There is no motivation to modify the device of Shibasaki”; “one of ordinary skill in the art would not be motivated to replace the Shibasaki buffer layer with the Ishikawa buffer layer, as the super lattice buffer layer of Ishikawa, which does not have a simple structure”; and “there is no motivation to modify Shibasaki by replacing the required simple buffer layer with the super-lattice required by Ishikawa”. However, in response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.d. 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.d. 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, the applicant made the erroneous assumption that the motivation to combine must be expressly stated in the art of record. From MPEP § 2144:

"The rationale to modify or combine the prior art does not have to be expressly stated in the prior art; the rationale may be expressly or impliedly contained in the prior art or it may be reasoned from knowledge generally available to one of ordinary skill in the art, established scientific principles, or legal precedent established by prior case law. In re

Fine, 837 F.d. 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); *In re Jones*, 958 F.d. 347, 21 USPQ2d 1941 (Fed. Cir. 1992). See also *In re Eli Lilly & Co.*, 902 F.d. 943, 14 USPQ2d 1741 (Fed. Cir. 1990) (discussion of reliance on legal precedent); *In re Nilssen*, 851 F.d. 1401, 1403, 7 USPQ2d 1500, 1502 (Fed. Cir. 1988) (references do not have to explicitly suggest combining teachings); *Ex parte Clapp*, 227 USPQ 972 (Bd. Pat. App. & Inter. 1985) (examiner must present convincing line of reasoning supporting rejection); and *Ex parte Levengood*, 28 USPQ2d 1300 (Bd. Pat. App. & Inter. 1993) (reliance on logic and sound scientific reasoning)." [Emphasis added]

In the present case, the examiner has presented a line of reasoning supporting his motive to combine which was expressly stated in the rejection in the last office action and is expressly stated in the rejection below. The applicant cannot rebut the examiner's arguments simply by making the inaccurate statement that the examiner has provided no line of reasoning for the applicant to rebut. Moreover, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

It is argued, at page 14 of the remarks, that "non of the presently cited references (Shibasaki and Ishikawa), taken alone or together, disclose, teach or suggest a high power semiconductor device including an active layer having a high power active element formed therein". However, lines 41,42, column 16; and lines 37,38, column 17; lines 4,5, column 19, figs. 3,14 of Shibasaki et al. does show a high power semiconductor FET device for a radio communication system having an active layer 3 formed on the buffer layer 2 and having a high

power active element (FET) for radio communication formed therein. Thus, Applicant's claims 1-10 do not distinguish over Shibasaki et al. and Ishikawa references.

Conclusion

3. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a). A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

4. Any inquiry concerning this communication or earlier communication from the examiner should be directed to Tan Tran whose telephone number is (571) 272-1923. The examiner can normally be reached on M-F 8:30AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306 for regular communications and (703) 872-9306 for after final communications.

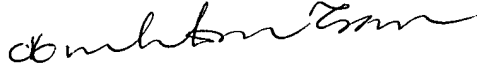
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Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

TT

May 2004


Minhloan Tran
Primary Examiner
Art Unit 2826